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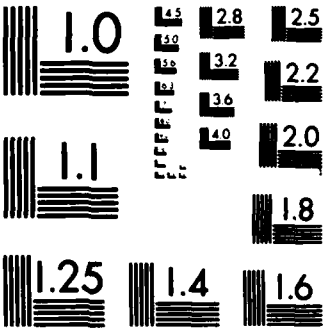

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Research in Monolithic Signal-Processing Circuits

R. G. Meyer and D. O. Pederson

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

A new wideband, low-noise bipolar current amplifier has been devised, fabricated and tested. A bandwidth of 184 MHz and input noise of 46 nA rms were achieved. A new low-noise wideband NMOS pre-amplifier was synthesized, fabricated and tested. This yielded 750 MHz bandwidth with 5.5 dB noise figure. New techniques were generated for the realization of very general MOS programmable function synthesizers.

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Research Results

Research supported under this grant led to eight major publications and the project has resulted in three completed Ph.D. dissertations, six M.S. reports and one U.S. patent.

A major research project under this program has been the synthesis of new wideband monolithic amplifier topologies. A new circuit was generated for wideband (up to 1 GHz and beyond) low current-noise amplifiers [13]. Unlike existing configurations, the topology is inherently tolerant of input node capacitive loading and is ideally suited to applications such as wideband fiber-optic communication receivers and wideband nuclear particle detectors. Design equations were derived which allow tradeoff of bandwidth, gain and noise in particular applications. A test amplifier was designed and fabricated in a 6 GHz Si bipolar monolithic process and yielded bandwidth and input noise current of 184 MHz and 46 nA rms respectively. These were close to predicted values. Further, computer simulation based on a 6 GHz fabrication process showed ready extension of this technique to 1 GHz operation. The use of more advanced processing (f_T = 10 GHz) extends the application of this circuit to signal frequencies beyond 2 GHz.

Our research in monolithic wideband amplifiers has also been applied to MOS realizations. A major thrust of all our research is the synthesis of techniques which are generally applicable to any technology followed by the reduction to practice in particular forms to verify the results and to

delineate practical differences between technologies. This also allows us to suggest future directions for technology research and development. In the case of MOS wideband circuits, we began by examining new methods for realizing very fast comparators and associated wideband pre-amplifiers. Practical applications for such circuits include fast data receivers where dense MOS digital circuits could be fabricated on the same integrated circuit as the analog input elements. We fabricated experimental MOS comparator circuits having 4 bits of resolution at 750 Ms/s and associated MOS pre-amplifiers with 1.25 GHz bandwidth [11]. This work illustrated the potential of very-high-frequency MOS circuits and further research in this area has resulted in a new low-noise MOS pre-amplifier configuration in a 1.5 μm process yielding measured noise figure of 5.5 dB in a 50 Ω sytem with 750 MHz bandwidth and 17 dB gain [17]. Computer simulations show that 4 dB noise figure and 1.3 GHz bandwidth are possible using existing MOS technologies. These circuits were optimized to take advantage of MOS device characteristics and as such are almost directly applicable to GaAs FET realization with consequent increases in operating speed.

Our research in MOS circuits has also been directed towards lower frequency signal-processing functions. We devised new techniques for nonlinear function synthesis using analog MOS monolithic circuits. The first application of these techniques was the realization of an MOS triangle-to-sine wave converter. The circuit included full compensation for temper-

ature and processing tolerances and an experimental monolithic test chip generated sine waves with 0.2% total harmonic distortion over a wide temperature range with a bandwidth of 1.1 MHz [10]. This research led to the generation of new techniques for the realization of very general MOS programmable function synthesizers [18].

A monolithic version of the function synthesizer was fabricated, and the task of correcting the nonlinearity of the FM transfer characteristic of a high-frequency voltage-controlled crystal oscillator was chosen as an appropriate test. The resulting measured transfer characteristic showed errors less than 2.3% over 100 °C temperature range. This work demonstrates the practicality of explicit monolithic nonlinear analog function synthesizers based on the nonlinear device characteristics of the MOSFET.

Other areas of research include nonlinear electronic functions in Si bipolar technology. We produced the first published theory of intermodulation in bipolar transistor mixers at high frequencies. The basic distortion mechanisms were identified and nonlinear equations describing the circuit operation were derived [12]. Measurements on bipolar double-balanced mixers at 100 MHz verified the theory, which allows designers to optimize device characteristics and bias conditions for minimum intermodulation and maximum dynamic range at frequencies up to the device f_T. These techniques can be applied to the prediction of intermodulation in FET mixers using either MOS or GaAs technology.

Finally, our research in high-frequency monolithic voltage-controlled oscillators (VCO) and phase-locked loops has resulted in the synthesis of new topologies with much improved performance over existing circuits. We fabricated a text VCO with temperature coefficient of center frequency better that 50 ppm/°C over frequencies from 1–200 MHz. A new digital frequency-detector circuit was devised which greatly improves the frequency acquisition capability of monolithic phase-locked loops.

Publications and Dissertations

A. Ph.D. Dissertations

1. D. Soo, "High Frequency Voltage Amplification in MOS Technology," 1985.

2. J. Fattaruso, "Nonlinear Analog Function Synthesis with MOS Technology," 1986.

3. K. Toh, "Wideband, Low-Noise Matched Impedance Amplifiers in Submicron MOS Technology," 1986.

B. M.S. Reports

4. R. Tsang, "A High-Frequency CMOS VCO," 1985.

5. E. Siu, "A Monolithic Wideband Variable Gain Amplifier," 1985.

6. G. Madine, "A Monolithic 50 MHz Phase-Locked Loop for Timing Recovery," 1984.

7. K. Kundert, "A Switched-Capacitor Synchronous Detector," 1983.

8. B. Lai, "Amplification Beyond f_T Using Non-Inductive Techniques," 1983.

9. J. Fattaruso, "MOS Current-Controlled Oscillators," 1983.

C. Publications Under Grant DAAG29-84-K-0043

10. J. Fattaruso and R. G. Meyer, "Triangle-to-Sine Wave Conversion with MOS Technology," *IEEE J. Solid-State Circuits*, Vol. SC-20, No. 2, April 1985, pp. 623–631.

11. D. Soo et. al., "A 750 Ms/s NMOS Latched Comparator," *IEEE ISSCC Digest*, Vol. 28, February 1985, pp. 146–147.

12. R. G. Meyer, "Intermodulation in High-Frequency Bipolar Transistor Integrated-Circuit Mixers," *IEEE J. Solid-State Circuits*, Vol. SC-21, No. 4, August 1986, pp. 534–537.

13. R. G. Meyer and R. A. Blauschild, "A Wideband Low Noise Monolithic Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, Vol. SC-21, No. 4, August 1986, pp. 530–533.

14. R. G. Meyer and R. S. Muller, "Charge-Control Analysis of the Collector-Base Space-Charge Region Contribution to Bipolar Transistor Time Constant τ_T," *IEEE Trans. on Electron Devices*, Vol. ED-34, No. 2, February 1987, pp. 450–452.

15. J. Santos and R. G. Meyer, "A One-Pin Crystal Oscillator for VLSI Circuits," *IEEE J. Solid-State Circuits*, Vol. SC-19, No. 2, April 1984, pp. 228–236.

16. J. Santos and R. G. Meyer, "One Pin Crystal Oscillator," U.S. Patent 4,600,898, July 15, 1986.

17. K. Y. Toh, et. al., "A Matched Impedance NMOS Amplifier," *IEEE ISSCC Digest*, February 1987, pp. 168–169.

18. J. Fattaruso and R. G. Meyer, "Nonlinear Analog Function Synthesis with MOS Technology," *IEEE CICC Digest*, 1987, pp. 647–650.

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